IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS

FLASH-CONTROL, LLC Plaintiff, v. INTEL CORPORATION Defendant.	**Civil Action No. 6:20-cv-360** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Flash-Control, LLC ("Flash-Control" or "Plaintiff"), for its Complaint against Defendant Intel Corporation (referred to herein as "Intel" or "Defendant"), alleges the following:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

THE PARTIES

2. Plaintiff Flash-Control is a limited liability company organized under the laws of the State of Delaware, and its registered agent for service of process in Delaware is Rita Carnavale, 717 North Union Street, Wilmington, Delaware, 19805.

3. Upon information and belief, Intel is a corporation organized under the laws of the Delaware with a place of business at 220 Mission College Blvd., Santa Clara, California, 95054, and with offices at 1300 S MoPac Expressway, Austin, Texas, 78746. Upon information and belief, Intel sells, offers to sell, and/or uses products and services throughout the United States, including in this judicial district, and introduces infringing products and services into the stream

of commerce knowing that they would be sold and/or used in this judicial district and elsewhere in the United States.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code.

5. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

6. Venue is proper in this judicial district under 28 U.S.C. § 1400(b).

7. This Court has personal jurisdiction over Intel under the laws of the State of Texas, due at least to their substantial business in Texas and in this judicial district, directly or through intermediaries, including: (i) at least a portion of the infringements alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in the State of Texas. Venue is also proper in this district because Intel has a regular and established place of business in this district. For instance, Intel has research, development, and corporate offices in this judicial district. For example, Intel has research, development, and corporate office located at 1300 S MoPac Expressway, Austin, Texas, 78746. (*See, e.g.*, https://www.intel.com/content/www/us/en/location/usa.html.)

BACKGROUND

The Invention

8. Mohan Rao is the inventor of U.S. Patent Nos. 9,257,184 ("the '184 patent") and 9,792,219 ("the '219 patent"). A true and correct copy of the '184 patent is attached as Exhibit A. A true and correct copy of the '219 patent is attached as Exhibit B.

9. The '184 and '219 patents resulted from the pioneering efforts of Dr. Rao (hereinafter "the Inventor") in the area of nonvolatile memory systems. These efforts resulted in

development and patent applications entitled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES" with development starting in the early 1990s. At the time of these pioneering efforts, the most widely implemented technology used to address the access time to data stored in nonvolatile memory was flash memory. In that type of system, the read and write access was slow compared volatile memory. The Inventor conceived of the inventions claimed in the '184 and '219 patents as a way to enhance the access to data stored to nonvolatile memory.

10. For example, the Inventor developed a nonvolatile memory system to decrease the amount of time it takes to access information from the nonvolatile memory.

Advantage Over the Prior Art

11. The embodiments described by the '184 and '219 patents, provides many advantages over the prior art, and in particular improve the operations of accessing data within stored within a nonvolatile memory system. (*See* '219 patent at Abstract and '219 patent at Figure 1.) One advantage of the patented invention is decreasing retrieval time of data stored within a nonvolatile memory system. (*See* '184 patent at 4:37-43.)

12. Another advantage is enhanced read and write performance of the memory system. (*See* '184 patent at Abstract.)

13. Another advantage is enhancing the random access performance of nonvolatile IC, subsystem and system. (*See* '184 patent at 1:61-63.)

14. Yet another advantage is decreased latency. (*See* ''219 patent at 4:46-49.)

15. Because of these significant advantages that can be achieved through the use of the embodiments of the '219 patent, Flash-Control believes that the '184 and '219 patents presents significant commercial value for companies like Intel. Indeed, Intel's Optane and

NVDIMM technology are widely used to provide access to data stored within a nonvolatile memory system.

Technological Innovation

16. The embodiments disclosed in the '184 and '219 patents resolve technical problems related to nonvolatile memory storage systems, particularly problems related to the utilization of memory stored in nonvolatile memory. As the '184 and '219 patents explain, one of the limitations of the prior art regarding nonvolatile memory storage systems was that the performance time including the read time, program/write time is slow compared to volatile memory system built with SRAMs and DRAMs. (*See* '219 patent at 1:56-58.)

17. The claims of the '184 and '219 patents do not merely recite the performance of some well-known business practice from the pre-Internet world along with the requirement to perform it on the Internet. Instead, the claims of the '184 and '219 patents recite inventive concepts that are deeply rooted in engineering technology, and are directed to problems specifically arising out of how to decrease the amount of time required to retrieve data stored in nonvolatile memory.

18. In addition, the claims of the '184 and '219 patents are directed to inventive concepts that improve the functioning of a nonvolatile memory system particularly improving accessibility of stored data.

19. Moreover, the claims of the '184 and '219 patents are directed to inventive concepts that are not merely routine or conventional use of nonvolatile memory. Instead, the patented inventions of the '184 and '219 patents are directed to a new and novel solution to specific problems related to improving nonvolatile memory storage systems.

20. And finally, the claimed invention of the ’184 and ‘219 patents do not preempt all the ways that nonvolatile memory systems, nor do the ’184 and ‘219 patent preempt any other well-known or prior art technology.

21. Accordingly, the claims in the ’184 and ‘219 patents recite a combination of elements sufficient to ensure that the claims in substance and in practice amount to significantly more than a patent-ineligible abstract idea.

COUNT 1 – INFRINGEMENT OF U.S. Patent No. 9,357,184

22. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief – Count 1.

23. On February 9, 2016, the ’184 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES”

24. Flash-Control is the assignee and owner of the right, title and interest in and to the ’184 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

25. Upon information and belief, Intel has infringed and continues to directly infringe one or more claims of the ’219 patent by selling, offering to sell, making, using (including without limitation testing), importing and/or providing and causing to be used products, specifically one or more Optane and nonvolatile dual in-line memory module (NVDIMM) based products, which by way of example include https://www.intel.com/content/www/us/en/architecture-and-technology/optane-dc-persistent-memory.html (the “Accused Instrumentalities”). The “Accused Instrumentalities” include but

are not limited to Intel Optane DC 512 GB Persistent Memory Module, Intel Optane DC 128 GB Persistent Memory Module, and Intel Optane DC 256 GB Persistent Memory Module.

26. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time required to access data stored in the nonvolatile memory.

27. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system such as an Intel Optane technology including a non-NAND, non-volatile storage media. *See* Claim Chart for the '184 Patent, attached hereto as Exhibit C.

28. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage of digital information in addressable locations arranged in multiple blocks for access. Including 3D XPoint Memory, a nonvolatile memory with 11 chips, 8 for data, wherein after the request is translated, the actual access to storage media occurs. The Optane DC's internal block size is 256 B. *Id.*

29. Upon information and belief, one or more of the Accused Instrumentalities includes requiring writing of modified digital information into a new physical location mapped to the same associated addressable location when reading any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location. Including translating an address after a request reaches the control; and accessing the storage media after a request is translated wherein the write amplification occurs as smaller stores issued by the CPU and is handled as read-modify-write operations. Additionally, controller performs housekeeping on the module, including wear leveling. *Id.*

30. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory for read and write operations. Including a DRAM and an XPController with a write-combining buffer. *Id.*

31. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory coupled to nonvolatile memory for storage controlled by one or more controllers. Including, a controller to perform housekeeping functions, such as wear leveling and managing data into and out of the 3D XPoint Memory. Memory accesses to the NVDIMM arrive at the controller which coordinates access to the 3D XPoint media. *Id.*

32. Upon information and belief, one or more of the Accused Instrumentalities has one or more controllers controlling the volatile and nonvolatile memories to perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block and the associated addressable location wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory. Including translating the address after the access request reaches the controller. After the request translation occurs, the actual access to storage media occurs. Such that, write amplification occurs as smaller stores issued by the CPU are handled as read-modify-write operations by the controller. The first cache line access loads the entire XPLine into XPBuffer, and the following three accesses read data in the buffer. The reads also compete for space in the XPBuffer. In response to receiving a read request of 64 bytes of data the module copies a block of 256 bytes, XPLine, from the 3D XPoint media to the XPBuffer. The requested 64 bytes are accessible from the XPBuffer. *Id.*

33. Upon information and belief, one or more of the Accused Instrumentalities performs a read operation from the volatile memory of any portion or all of the stored digital

information in the volatile memory. Including, a first cache line access that loads the entire XPLine (a block of 256 bytes of data) into XPBuffer, and the following three accesses read data in the buffer. The requested bytes are accessible from the XPBuffer. *Id.*

34. Upon information and belief, one or more of the Accused Instrumentalities performs a write operation of any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein. Including, read-modify-write operations on Optane DC memory by the controller.

35. Upon information and belief, one or more of the Accused Instrumentalities writes the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read. Including a controller on the Optane DIMM performing wear leveling. *Id.*

36. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 1 of the ’184 patent during the pendency of the ’184 patent.

37. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system coupled to a central processing unit. Including a persistent memory that is delivered with the next-generation processor. *Id.*

38. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 2 of the ‘184 patent during the pendency of the ‘184 patent.

39. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage is a phase change memory. *Id.*

40. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 4 of ‘184 patent during the pendency of the ‘184 patent.

41. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage is magnetic memory. *Id.*

42. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 5 of '184 patent during the pendency of the '184 patent.

43. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory is a SRAM with at least one port for read and write access. *Id.*

44. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 8 of '184 patent during the pendency of the '184 patent.

45. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory is a dynamic random access memory with at least one port for read and write access. *Id.*

46. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 9 of '184 patent during the pendency of the '184 patent.

47. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory with a pseudo static RAM with at least one port for read and write access. *Id.*

48. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 10 of '184 patent during the pendency of the '184 patent.

49. Upon information and belief, one or more of the Accused Instrumentalities includes each block of nonvolatile memory for storage has one or more pages of stored data accessible through the coupled volatile random access memory. *Id.*

50. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 11 of '184 patent during the pendency of the '184 patent.

51. Upon information and belief, one or more of the Accused Instrumentalities includes pages that are randomly addressable and accessible. *Id.*

52. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 12 of '184 patent during the pendency of the '184 patent.

53. Upon information and belief, one or more of the Accused Instrumentalities includes pages that are serially addressable and accessible. *Id.*

54. One or more of the Accused Instrumentality infringed and continue to infringe at least claim 14 of '184 patent during the pendency of the '184 patent.

55. Upon information and belief, one or more of the Accused Instrumentalities includes each page of a block can be substituted on the fly for any other page of a different block through address mapping. *Id.*

56. One or more of the Accused Instrumentality infringed and continue to infringe at least claim 15 of '184 patent during the pendency of the '184 patent.

57. Upon information and belief, one or more of the Accused Instrumentalities includes each of the randomly addressable and accessible pages is capable of addressing at least one bit in each access. *Id.*

58. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 16 of '184 patent during the pendency of the '184 patent.

59. On information and belief, the above identified infringement has been and continues to be willful.

60. Flash-Control has been harmed by the above identified infringing activities.

COUNT 2 – INFRINGEMENT OF U.S. PATENT NO. 9,792,219

61. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief – Count 2.

62. On October 17, 2017, the ’219 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE.”

63. Flash-Control is the assignee and owner of the right, title and interest in and to the ’219 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

64. Upon information and belief, Intel has infringed and continues to directly infringe one or more claims of the ’219 patent by selling, offering to sell, making, using (including without limitation testing), importing and/or providing and causing to be used products, specifically one or more Optane and nonvolatile dual in-line memory module (NVDIMM) based products, which by way of example include https://www.intel.com/content/www/us/en/architecture-and-technology/optane-dc-persistent-memory.html (the “Accused Instrumentalities”). The “Accused Instrumentalities” include but are not limited to Intel Optane DC 512 GB Persistent Memory Module, Intel Optane DC 128 GB Persistent Memory Module, and Intel Optane DC 256 GB Persistent Memory Module.

65. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time required to access data stored in the nonvolatile memory.

66. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system such as a non-volatile dual in-line memory module (NVDIMM) *See* Claim Chart for the ‘219 Patent, attached hereto as Exhibit D.

67. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage of digital information arranged in multiple blocks for access. Including a non-volatile memory (NVM) where access to storage happens in blocks. *Id.*

68. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory for read and write operation couple to said nonvolatile memory. Including, an NVDIMM-N with a flash memory and traditional DRAM in one module wherein data can be copied from DRAM to flash memory, supporting both block addressing and traditional DRAM-like byte addressing. *Id.*

69. Upon information and belief, one or more of the Accused Instrumentalities has a volatile random access memory and nonvolatile memory controlled by one or more controllers. Including a NVMDIMM-N, a DRAM, and a NVDIMM Controller. *Id.*

70. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system coupled to a central processing unit. Including, a NVDIMM-P that combines the features of DRAM and flash with a CPU that can directly access the data. *Id.*

71. Upon information and belief, one or more of the Accused Instrumentalities includes each block of the nonvolatile memory for storage having one or more pages of stored data accessible through the coupled volatile random access memory, and each page of a block is adapted to be substituted on the fly for any other page of a different block through addressing mapping. Including an application that memory maps a file in the block access, the file system fetches those blocks from the device and stores them in DRAM. *Id.*

72. Upon information and belief, one or more of the Accused Instrumentalities has one or more controller control the volatile and nonvolatile memory to perform a read operation

on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location. Including a persistent memory and Asynchronous DRAM Refresh (ADR) with a memory controller with read and write operations in the block access. Including I/O requests that may be made in blocks of a predetermined size. *Id.*

73. Upon information and belief, one or more of the Accused Instrumentalities performs a read operation from the volatile memory of any portion or all of the store digital information in the volatile memory. Including reading blocks from DRAM. *Id.*

74. Upon information and belief, one or more of the Accused Instrumentalities preforms a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein. Including copying data to an intermediate DRAM buffer in userspace. *Id.*

75. Upon information and belief, one or more of the Accused Instrumentalities writes the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read. Including writing blocks from DRAM to a storage media. *Id.*

76. One or more of the Accused Instrumentality infringed and continue to infringe at least claim 1 of the ’219 patent during the pendency of the ’219 patent.

77. On information and belief, the above identified infringement has been and continues to be willful.

78. Flash-Control has been harmed by the Intel’s infringing activities.

JURY DEMAND

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Flash-Control demands a trial by jury on all issues triable as such.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Flash-Control demands judgment for itself and against Intel as follows:

A. An adjudication that Intel has infringed the '184 and '219 patents;

B. An award of damages to be paid by Intel adequate to compensate Flash-Control for Intel's past infringement of the '184 and '219 patents, and any continuing or future infringement through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

C. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of Flash-Control's reasonable attorneys' fees; and

D. An award to Flash-Control of such further relief at law or in equity as the Court deems just and proper.

Dated: May 4, 2020

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